400G QSFP-DD SR8 Optical Transceiver

Product Features

- Compliant with IEEE 802.3cm 400GBASE-SR8 specification
- Compliant with QSFP-DD MSA and CMIS 4.0
- 8x26.5625GBd PAM4 transmitter and PAM4 receiver
- 8 channels 850nm VCSEL array
- 8 channels PIN photo detector array
- Single +3.3V power supply
- Power consumption < 12W
- Operation case temperature: 0~70°C
- Standard Optical fiber with MPO-16 APC optical connector
- Maximum link length of 70m on OM3 MMF and 100m on OM4 MMF with FEC
- RoHS6 compliant

Applications

- 400G Ethernet
- InfiniBand interconnects
- Data center and enterprise networking

Absolute Maximum Ratings

Parameter	Unit	Min.	Typical	Max.	Notes
Storage Temperature	°C	-40		85	
Operating Relative Humidity	%	0		85	
Power Supply Voltage	V	-0.5		3.63	
Damaged Input Optical power	dBm	3			

Recommended Operating Conditions

Parameter	Unit	Min.	Typical	Max.	Notes
Operating Case Temperature	℃	0		70	1
Power Supply Voltage	V	3.135	3.3	3.465	
Power Supply Current	A			3.6	
Power Consumption	W			12	
Pre-FEC Bit Error Ratio			2.4E-4		2
Post-FEC Bit Error Ratio			1E-12		2
Bit Rate	Gbps		400		

Note：

1. Case Temperature here is depending on module case around TOSA, please do remember it is NOT the environmental temperature.
2. FEC is provided by host system.

Electrical Characteristics

Parameter	Unit	Min.	Typical	Max.	Test point[1]	Notes
Transmitter						
Signaling Rate per lane (range)	GBd	26.5625 ± 100 ppm			TP1	
Differential pk-pk Input Voltage Tolerance	mVpp	900			TP1a	2
Differential Input Return Loss	dB	Equation (83E-5)			TP1	
Differential to Common Mode Input Return Loss	dB	Equation (83E-6)			TP1	
Differential Termination Mismatch	%			10	TP1	
Module Stressed Input Test		See 120E.3.4.1			TP1a	3
Single-ended Voltage Tolerance Range	V	-0.4		3.3	TP1a	
DC Common Mode Voltage	mV	-350		2850	TP1	4
Receiver						
Signaling Rate per lane(range)	GBd	26.5625 ± 100 ppm			TP4	
Peak-to-peak Differential Output Voltage	mVpp			900	TP4	
AC Common-Mode Output Voltage, RMS	mV			17.5	TP4	
Differential Output Return Loss		Equation (83E-2)			TP4	
Common to Differential Mode Conversion		Equation (83E-3)			TP4	
Differential Termination Mismatch	%			10	TP4	
Transition Time, 20% to 80%	ps	9.5			TP4	
Near-end ESMW (Eye Symmetry Mask Width)	UI		0.265		TP4	
Near-end Eye Height, Differential	mV	70			TP4	
Far-end ESMW (Eye Symmetry Mask Width)	UI		0.2		TP4	
Far-end Eye Height, Differential	mV	30			TP4	
Far-end Pre-cursor ISI Ratio	%	-4.5		2.5	TP4	
DC Common Mode Voltage	mV	-350		2850	TP4	4

Notes:

1. The location of TP1, TP1a and TP4 are defined in IEEE 802.3bs Figure 120E–5 and Figure 120E–6.
2. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
3. Meets BER specified in IEEE 802.3bs 120E.1.1.
4. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

Optical Characteristics

All performance is defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Unit	Min.	Typical	Max.	Note
Transmitter					
Signaling rate, each lane	GBd	26.5625 ± 100 ppm			
Modulation Format		PAM4			
TX Central Wavelength	nm	840	850	860	
Spectral Width (RMS)	nm			0.6	1
Average Launch Power, each lane	dBm	-6		4	
Outer Optical Modulation Amplitude (OMAouter), each lane	dBm	-4		3	2
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	dB			4.5	
Average Launch Power Tx_off	dBm			-30	
Extinction Ratio	dB	3			
Optical Return Loss Tolerance	dB			12	
$RIN_{12}OMA$	dB/Hz			-128	
Encircled Flux		>86% at 19 um <30% at 4.5 um			3
Receiver					
Signaling Rate, each lane	GBd	26.5625 ± 100 ppm			
Modulation Format		PAM4			
RX Central Wavelength	nm	840	850	860	
Damage Threshold (min)	dBm	5			4
Average Receive Power each lane	dBm	-8.4		4.0	5
Receive Power (OMAouter) each lane	dBm			3	
Receiver Reflectance	dB			-12	
Stressed Receiver Sensitivity (OMAouter) each lane	dBm			-3.4	6
Receiver sensitivity (OMAouter), each lane		Equation (138–1)			7
Conditions of Stressed Receiver Sensitivity Test:					8
Stressed Eye Closure for PAM4 (SECQ), lane under test	dB			4.5	
SECQ – $10\log10(C_{eq})f$, each lane	dB			4.5	9
OMAouter of each Aggressor Lane	dBm			3	
LOS Assert	dBm	-20			
LOS De-Assert	dBm			-8	
LOS Hysteresis	dB	0.5			

Notes:

1. RMS spectral width is the standard deviation of the spectrum.
2. Even if the TDECQ ＜ 1.4 dB, the OMA (min) must exceed this value.
3. If measured into type A1a.2 or type A1a.3, or A1a.4, 50 µm fiber, in accordance with IEC 61280-1-4.
4. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.
5. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
6. Measured with conformance test signal at TP3 (see IEEE802.3cd-2018 138.8.10) for the BER specified in 138.1.1.
7. Receiver sensitivity is informative and is defined for a transmitter with a value of SECQ up to 4.5 dB.

   RS = max(6.5 – SECQ–7.9) (dBm) Equation (138–1)

   where

   RS is the receiver sensitivity

   SECQ is the SECQ of the transmitter used to measure the receiver sensitivity.

   The normative requirement for receivers is stressed receiver sensitivity.

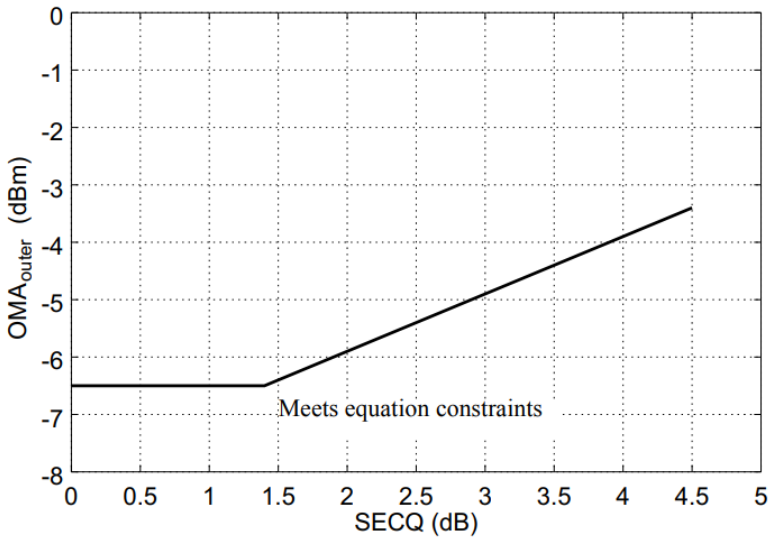
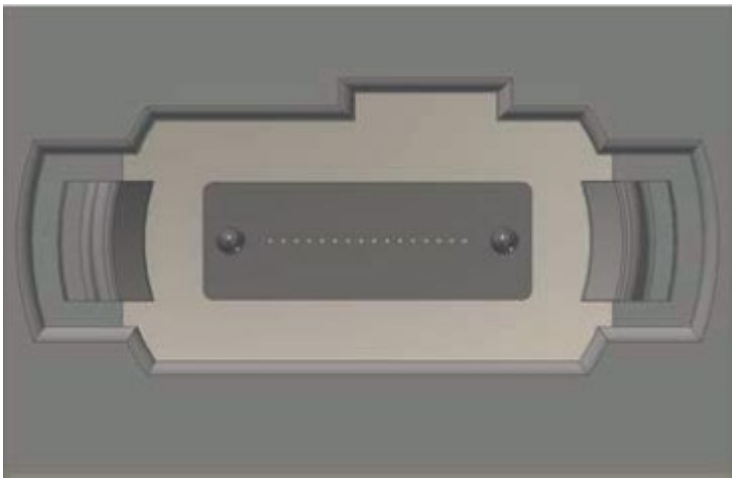


Figure1: Illustration of receiver sensitivity

8. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.
9. C_{eq} is a coefficient defined in IEEE802.3bs 121.8.5.3, which accounts for the reference equalizer noise enhancement.

Optical Interface



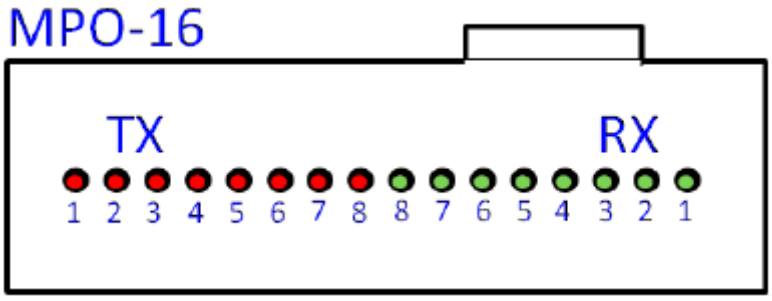
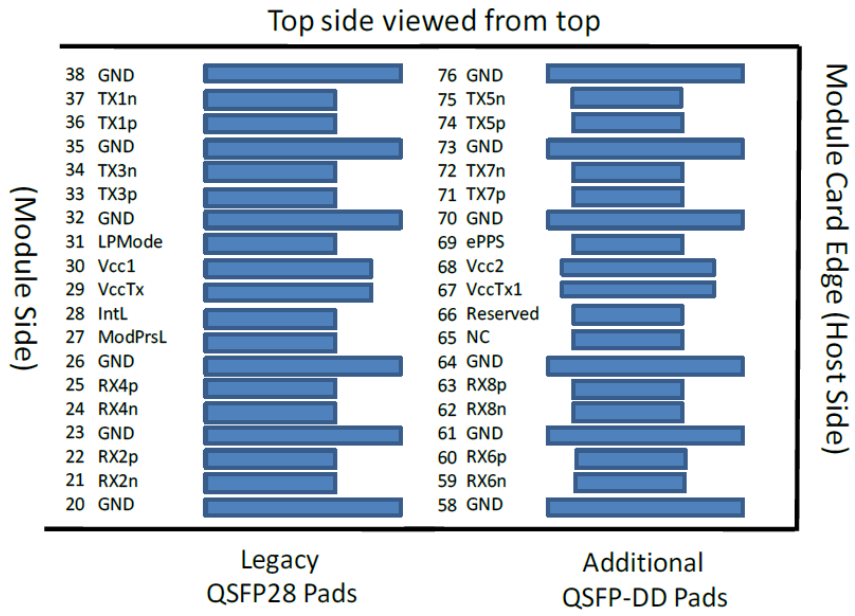


Figure 2: MPO-16 Single Row optical patch cord and module receptacle

Pin Assignment and Description



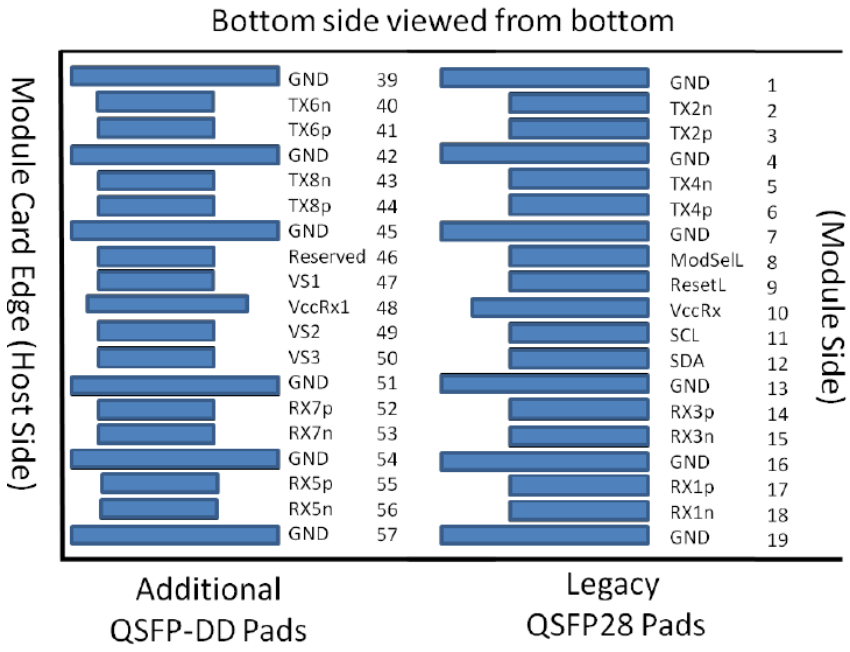


Figure 3： Module pad layout

PIN Definition

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1

21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	

60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Notes:

1. QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 3 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

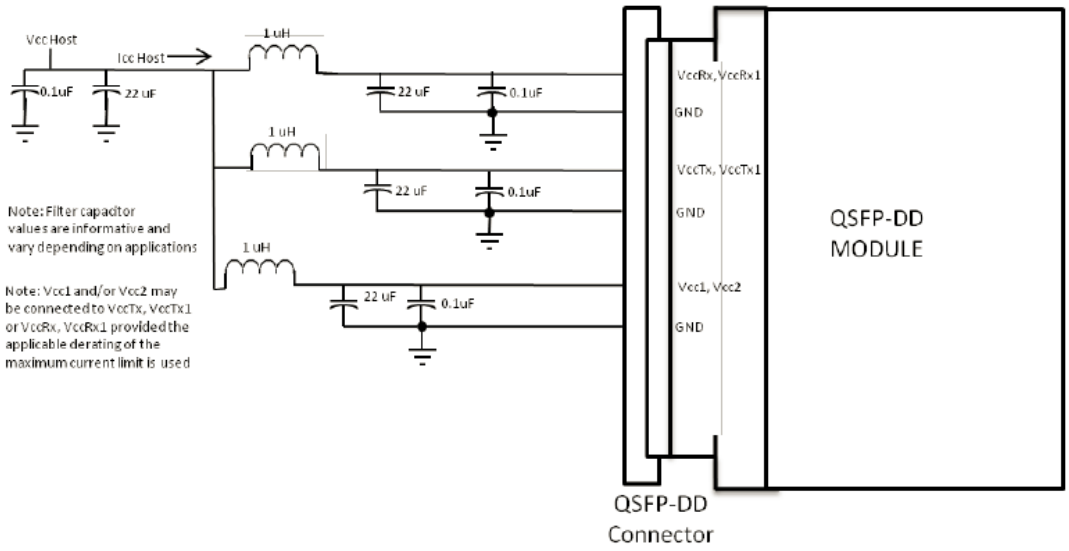


Figure 4: Recommended Host Board Power Supply Filtering

OUTLINES

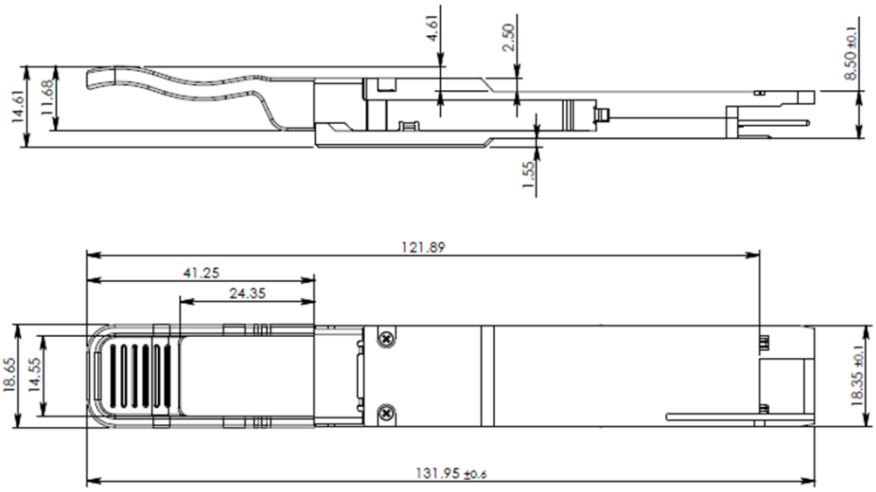
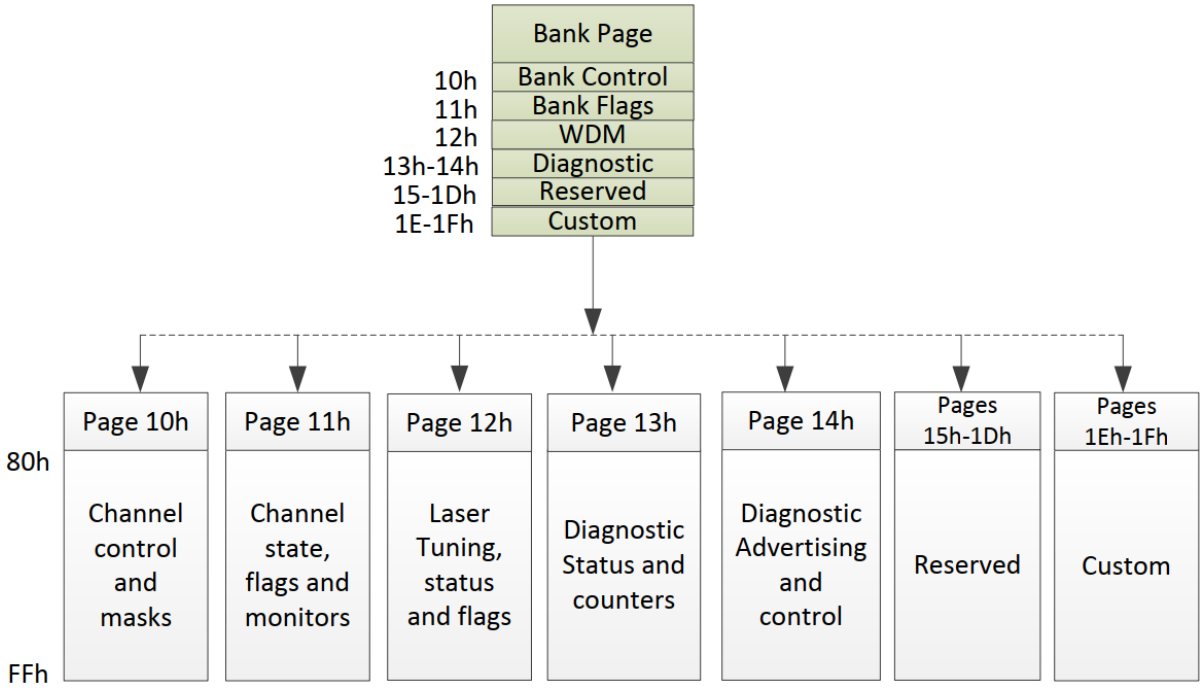


Figure 5: Mechanical Outline

Digital Diagnostic Functions

Parameter	Units	Error	NOTES
Temperature Monitor	°C	±3	1LSB=1/256°C
Supply Voltage Monitor	V	±0.1	1LSB=100uV
Bias Current Monitor	mA	±10%	1LSB=2uA
TX Power Monitor	dB	±3	1LSB=0.1uW
RX Power Monitor	dB	±3	1LSB=0.1uW



ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Laser Safety

This is a Class 1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

Ordering Information

Ordering P/Ns	Description
DH88mm-MMCA	8x53G QSFP56-DD SR8, 850nm, MMF, MPO, Commercial temperature.

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